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## Abstract of the Disclosure

A circuit is provided for reducing mismatches between the outputs of successive pairs of cells in an analog to digital converter. A voltage input means is coupled to a first input terminal of each cell to introduce and an input voltage. A reference voltage means is coupled to a second input terminal of each cell to introduce progressive fractions of a reference voltage. A low impedance means is coupled between corresponding first output terminals and coupled between corresponding second output terminals in successive cells, to draw load-bearing currents to the successive cells, affecting the relative voltages and thereby reducing the effects of cell mismatches on these output terminals. Lastly, a high impedance means is coupled to the each of the first output terminals and to each of the second output terminals in successive cells.

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